Top Level View of Computer Function and Interconnection

Question 1: A microprocessor has an increment memory direct instruction, which adds 1 to the value in a memory location. The instruction has five stages:

- Fetch opcode (four bus clock cycles).
- Fetch operand address (three cycles).
- Fetch operand (three cycles).
- Add 1 to operand (three cycles).
- Store operand (three cycles).

a- Calculate the overall instruction cycles.
b- If we have to insert two bus wait cycles in each memory read and memory write operation, what is the amount of increasing in the instruction cycle?
c- Repeat (b) assuming that the increment operation takes 13 cycles instead of 3 cycles.

Question 2:

Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

a. What is the maximum directly addressable memory capacity (in bytes)?
b. Discuss the impact on the system speed if the microprocessor bus has
   1. a 32-bit local address bus and a 16-bit local data bus, or
   2. a 16-bit local address bus and a 16-bit local data bus.
c. How many bits are needed for the program counter and the instruction register?

Question 3:

3.1 The hypothetical machine of Figure 3.4 also has two I/O instructions:

0011 = Load AC from I/O
0011 = Store AC to I/O

In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 3.5) for the following program:

1. Load AC from device 5.
2. Add contents of memory location 940.
3. Store AC to device 6.

Assume that the next value retrieved from device 5 is 3 and that location 940 contains a value of 2.

3.2 The program execution of Figure 3.5 is described in the text using six steps. Expand this description to show the use of the MAR and MBR.

Question 4:

Consider a hypothetical microprocessor generating a 16-bit address (for example, assume that the program counter and the address registers are 16 bits wide) and having a 16-bit data bus.

a. What is the maximum memory address space that the processor can access directly if it is connected to a "16-bit memory"?
b. What is the maximum memory address space that the processor can access directly if it is connected to an "8-bit memory"?
c. What architectural features will allow this microprocessor to access a separate "I/O space"?
d. If an input and an output instruction can specify an 8-bit I/O port number, how many 8-bit I/O ports can the microprocessor support? How many 16-bit I/O ports? Explain.

Question 5:

a) Draw and explain the timing diagram of PCI
b) List and briefly define two methods to dealing with multiple interrupts?
c) Draw the instruction cycle state diagram with interrupts
d) What is the benefit of using a multiple-bus architecture compared to a single –bus architecture?
e) What are the groups of signal lines for the PCI (required and option)
f) What are the interrupts classes?